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| King Fahd University of Petroleum & Minerals |
| Department of Electrical Engineering |
| EE200: Digital Logic Circuit Design |
| Spring Semester 2015 (151) |

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| Week | Laboratory |
| 1 | No Lab. |
| 2 | Exp#1: Getting Started with the Laboratory Equipment |
| 3 | Exp#2: Building Logic Functions using Traditional ICs |
| 4 | No Lab. |
| 5 | No Lab. |
| 6 | Exp#3: Introduction to Verilog HDL and FPGA |
| 7 | Exp#4: Programming with Verilog HDL (Part I) |
| 8 | Exp#5: Programming with Verilog HDL (Part II) |
| 9 | Exp#6: Combinational Logic Circuits (Part I) |
| 10 | Exp#7: Combinational Logic Circuits (Part II) |
| 11 | Exp#8: Combinational Logic Circuits (Part III) |
| 12 | Exp#9: Sequential Logic Circuits (Part I) |
| 13 | Exp#10: Sequential Logic Circuits (Part II) |
| 14 | Exp#11: Final Lab Project |
| 15 | **Lab Final** |

* **Grade Policy**
  + Pre-labs 2
  + Report 3
  + Quizzes 4
  + Project 4
  + Final 7
* **Attendance**:
  + 2 absences (excused or non-excused) : Warning
  + 3 absences (non-excused): DN
  + 4 absences (excused or non-excused) : DN
  + -0.5 for each unexcused absence & -0.1 for every 5 minutes late will be deducted out of the student final grade.
* **Lab Performance**:
  + For students behaving carelessly and showing non-serious attitude during the lab, points will be deducted out of their final grade, on a per-experiment basis.

**Important Points to Remember**

1. No Lab. Makeup: No lab make-ups are allowed
2. No report accepted without lab: Lab report will not be accepted without performing the lab
3. Official excuses: All official excuses must be submitted to the instructor no later than one week of the date of the official excuse. The instructor may not accept the late excuses.